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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,857	08/06/2003	Toshio Arakawa	1081.1180	6516

21171 7590 06/16/2004

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)	
	10/634,857	ARAKAWA, TOSHIO	
	Examin r	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/634857 file on 08/06/03.

Claim 1-11 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Beausang et al. (US Patent 5949692).

4. As to claims 1, and 8, Beausang et al. teach a design method for an integrated circuit having a logic circuit, comprising: first step converting a first netlist, which has connection data for a logic circuit in which a plurality of standard cells including at least a first flip flop are connected, into a second netlist by converting the first flip flops into second flip flops equipped with a scan function and adding scan chain interconnects that connect the second flip flops (see fig 6-14 and col 10 line54 to col 11 lines 39); second step of generating a third netlipt second netlist a plurality of standard cells that constitute the second flip f lops, and generating scan-chain interconnect data (see fig 6-14 and col 11 lines 39 to col 13 lines 19); third step of performing layout of the standard cells and interconnects thereof which are contained in the third netlist, in accordance the third netlist, optimizing an order of the scan chain interconnects on the basis of the scan chain interconnect data, and generating scan-chain interconnect order data (see fig 1, and 6-14 and col 13 lines 21 to col 14 lines 40); and a fourth step of generating a fifth

netlist, from a fourth netlist that includes the second flip flops, and scan chain interconnects that depend on the scan-chain interconnect order data, by substituting the second flip flops for a plurality of standard cells, and of performing layout of the standard cells and interconnects thereof which are contained in the fifth netlist, in accordance with the fifth netlist (see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background).

5. As to claims 2, Beausang et al. teach further comprising: a step of generating logic circuit test patterns on the basis of the fourth netlist (see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background).

6. As to claims 3, Beausang et al. teach wherein the test patterns include an input test pattern that is inputted to the second flip flops the logic circuit, and an expected-value test pattern, which expected to be outputted by the second flops after a predetermined cycle operation (see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background and summary).

7. As to claims 4, Beausang et al. teach wherein the second flip flops and standard registered in a logic library that contains logic information, and reference is made the logic library in the test pattern generation step data (see fig 1, and 6-14 and col 13 lines 21 to col 14 lines 40).

8. As to claims 5 Beausang et al. teach wherein the fourth netlist is formed by converting the first flip flops contained in the first netlist into second flip flops and adding scan chain interconnects that depend on the scan-chain interconnect order data (see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background and summary).

9. As to claim 6, 9, and 10 Beausang et al. teach wherein the standard cells are registered a layout library as hard macros contain layout information, and the layout of the standard cells is

performed the fourth step with reference to layout library(see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background and summary).

10. As to claim 7, and 11 Beausang et al. teach wherein the second flip flop having the scan function is not registered in the layout library as hard macro that contains layout information (see fig 1, and 6-14 and col 11 lines 21 to col 14 lines 40 and background and summary).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
June 11, 2004

K. M. THOMPSON
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800